REMARKS

Claims 1, 4-6, 9-16 and 19-26 are pending in the application.

Claims 1, 4-6, 9-16 and 19-26 have been rejected.

Claims 4 and 9 have been canceled.

Claims 1, 5 and 11 have been amended.

New independent Claims 27 and 28 have been added. The support for the new claims can be found, for example, on pages 3-5 of the Applicant's disclosure.

I. REJECTIONS UNDER 35 U.S.C. § 103(a)

Claims 1, 4, 22-23 and 26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application Publication No. 2003/0142624 to *Chiussi* (hereinafter "Chiussi") in view of U.S. Patent Application Publication No. 2004/0136370 to *Moore* (hereinafter "Moore") and U.S. Patent Application Publication No. 2002/0085578 to *Dell* (hereinafter "Dell"). Claims 5-6 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiussi in view of Moore. Claim 10 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiussi in view of Moore as applied to claim 9 above, and further in view of U.S. Patent Application Publication No. 2003/0035422 to *Hill* (hereinafter "Hill"). Claims 11-16 and 19-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application Publication No. 2001/0033581 to *Kawarai* (hereinafter "Kawarai") in view of Chiussi, Moore and Dell. Claim 23 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiussi in view of Moore and Dell as applied to claim 1 above, and further in view of Hill. Claim 25 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiussi in view of Dell and Moore as applied to claim 1 above, and further in view of Kawarai. The rejections are respectfully traversed.

The Applicant's disclosure provides a system and method of simplying the scheduling of data routed through a data switch. In certain embodiments, contention free GT (guaranteed throughput) scheduling is performed in one step by reserving a connection between a data switch input and a data switch output. Therefore, the scheduling of both the input and output is done in one step. BE (best

effort) scheduling is then done also by reserving a connection between a data switch input and data switch output while using the GT reservations as boundary conditions. The scheduling for both the data switch inputs and data switch outputs is carried out by a central scheduling mechanism.

Chiussi describes a system of routing input links (201-1 to z) to output links (202-j to s) via a data switch. On the input side of a switch fabric, there are a plurality of Communication Link Interfaces (CLI) that each provide a single link to the switch fabric. Each of the input CLIs receives multiple links (eg. 201-1 to r) and a scheduler within the input CLI schedules the information received on these links onto a single output to switch fabric link 203. In this manner, the single output to switch fabric link 203 is used to transmit packets as determined by the scheduler.

The scheduler in the input CLI is not aware of the scheduling of any other input CLIs and does not take into consideration possible contention with the destination of the packets coming from the other CLIs. In other words, the input CLI is not concerned with scheduling for the output of the switch fabric and does nothing to prevent two input CLIs from sending a packet to the same output destination.

Once a packet is transmitted over link 203, the packet is routed by the switch fabric to an output destination in the form of a corresponding CLI on the output side of the switch fabric. The output CLI may receive several packets from several input CLIs at the same time. Chiussi does not describe that the input CLIs do anything to prevent this from happening. In order to prevent contention on the output side, the output CLIs provide queues to buffer the information received from multiple links, and then a scheduler within the output CLI schedules the information to be output from the switch via switch output link 202-j.

In Chiussi, information on links 201-1 to 201-r is received by the switch 101-1 and scheduled to be output on an input to switch fabric. On the output side of the switch, information received from the switch fabric over links 204 are first scheduled before being output from the switch 101-1 on link 202-j. The input scheduling and output scheduling are done separately.

Claim 1 has been amended to recite, "each data switch output having one and the same output buffer both configured to collect guaranteed throughput and best effort data."

As contention in Chiussi may occur at the input of the output CLI, the output CLI comprises multiple flow queues (figure 5) to ensure that data that arrives simultaneously is not lost while the data waits to be scheduled to the output of switch 101-1.

Although the Office Action suggests that the packet RAM 607 of Chiussi discloses this feature, the packet RAM 607 contains BE (best effort) data packet flow queues 505 and GB (guaranteed bandwidth) data packet flow queues 502 wherein the relative packets are stored. Therefore, although packet RAM 607 stores packets, it consists of multiple flow queues that buffer the respective packets separately (see paragraph 48 and 49 of Chiussi).

The data switch outputs of the present disclosure only receive a single piece of information at a time and, therefore, need not differentiate and separately store different data.

Chiussi also does not disclose the element of "a guaranteed throughput control means configured to control a guaranteed throughput data scheduling to schedule the guaranteed data in one step, wherein the one step comprises at least one reservation of a connection between one of said data switch input and of said data switch output."

In Chiussi, the scheduler of the input CLI schedules the output onto link 203. The input scheduler is not concerned with the destination of the output on link 203 as any contention at the output destination is dealt with at the output destination by the output CLI. The Office Action has indicated that figure 4 relates to this element. Figure 4 shows the scheduler outputting packets on an outgoing link. This figure refers to a scheduler within a CLI and as such the outgoing link corresponds to link 203 on the input side of the switch fabric. Claim 1 requires that the data switch to be between a data switch output and a data switch input. The outgoing link of Chiussi does not correspond to this.

Accordingly, the Applicant respectfully submits that amended Claim 1 is patentable over the cited references.

In addition, Chiussi requires data scheduling to take place at the input of a switch fabric and again at the output of the switch fabric in order to solve contention on both the input and output side of the switch fabric. Chiussi does this in order to allow a scheduler in a CLI to deal with the

complexity of scheduling both BE and GB data without having the added complexity of having to deal with scheduling at the output side.

In distinct contrast, embodiments of the present disclosure provide a GT (guaranteed throughput) and BE scheduling in a combined and central manner for all the inputs and outputs of a data switch. The embodiments do this by providing a reservation step for contention free GT scheduling and reserving a link between an input and output in order to prevent contention. This provides the advantages that additional scheduling circuitry need not be provided on the output side of a switch, and the circuitry is further reduced by having only a single output buffer for both GT and BE data. Furthermore, the latency of the switch is reduced as a connection between a data switch input and a data switch output is reserved, and, therefore, scheduling need not take place for both the input and the output of the switch.

Furthermore, as the data scheduling in Chiussi is intended to isolate the scheduling at the input and output sides in order to simplify the job required of each scheduler while embodiments of the present disclosure simplify the scheduling itself and provide a central scheduling mechanism, Chiussi in fact teaches away from the embodiments of the present disclosure.

The present disclosure is, therefore, fundamentally different from that of Chiussi and because Chiussi does not encourage the person of ordinary skill to significantly modify that invention and even teaches away from the present disclosure, the present disclsoure is non-obvious in view of Chiussi. Since the person of ordinary skill would have to modify Chiussi's invention fundamentally before applying Dell and Moore, and Dell and Moore do not encourage such a modification, the present disclosure is non-obvious also in view of Dell and Moore.

Independent Claims 5 and 11 also have been amended to recite elements analogous to the novel elements emphasized above in traversing the rejection of Claim 1 and, therefore, also are patentable over the cited references. Additionally, Claims 22-26, Claims 6 and 10, and Claims 12-16 and 19-21 depend from Claims 1, 5 and 11, respectively, and include all the elements of their respective base claims. As such, Claims 2, 6, 10, 12-16 and 19-26 also are patentable over the cited references.

II. CONCLUSION

As a result of the foregoing, the Applicant asserts that the remaining Claims in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *rmccutcheon@munckcarter.com.*

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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